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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,205	09/24/2003	Sarah E. Kim	ITL.1040US (P14807)	2630
21906	7590	06/29/2005	EXAMINER	
TROP PRUNER & HU, PC 8554 KATY FREEWAY SUITE 100 HOUSTON, TX 77024			ISAAC, STANETTA D	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/669,205

Applicant(s)

KIM ET AL.

Examiner

Stanetta D. Isaac

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-7,14 and 16-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14,16 and 17 is/are allowed.
- 6) ☒ Claim(s) 1,3-7 and 18-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

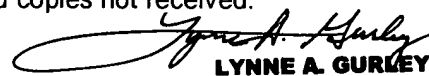
Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


LYNNE A. GURLEY

PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

This Office Action is in response to the RCE and amendment filed on 6/17/05.

Currently, claims 1, 3-7, 14 and 16-21 are pending.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/17/05 has been entered.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5 and 20 recites the limitation "lifting off a resist" in line1, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Jankowski et, al., Patent Application Publication US 2004/0072039.

Jankowski discloses the semiconductor method as claimed. See figures 1-11, and corresponding text, where Jankowski teaches a method comprising: forming a trench **906** (host structures) in each of two semiconductor substrates, at least one of said trenches extending completely across one of said semiconductor substrates from edge to edge (figures 5, 9 and 10; paragraphs [0023], [0025] and [0045-0046] *Note*: the Examiner takes the position that at least one of the trenches extend completely across at least one the semiconductor substrates, since Jankowski teaches, the substrates formed in a face-to-face abutment); providing a catalyst **904** in a trench (figures 9 and 10; paragraph [0044-0046]); and combining said substrates in a face-to-face abutment with said trenches (host structures) in alignment with one another (figures 9 and 10; paragraph [0029] and [0044-0046], *Note*: the Examiner takes the position that the substrates are in a face-to-face abutment, since Jankowski teaches, that the host structure consists of silicon wafers that have channels (implied trenches) etched within the silicon wafers, and are bonded together to form flow channels).

Pertaining to claim 6, Jankowski teaches the method including depositing the catalyst in the trench (figure 9; paragraph [0044]).

Pertaining to claim 7, Jankowski teaches the method including depositing platinum or lead in said trench (figure 9; paragraph [0045] platinum).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-5 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jankowski et al., Patent Application Publication US 2004/0072039 in view of Ramanathan et. al., Patent Application Publication US 2005/0003664.

Jankowski discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1, 6 and 7, under 35 U.S.C. 102(e). In addition, Jankowski shows, pertaining to claim 18, a method comprising: and defining a catalyst-filled **904** trench between said substrates (figures 9 and 10; paragraph [0044-0046]). Finally, Jankowski shows, pertaining to claim 21, including forming a trench in each of said semiconductor substrates ([0023], [0025] and [0045-0046]).

However, Jankowski fails to show, pertaining to claims 3 and 18, including combining said (two semiconductor substrates) substrates using copper-to-copper bonding. In addition, Jankowski fails to show, pertaining to claims 4 and 19, including masking said catalyst to avoid coating the catalyst with the copper. Also, Jankowski fails to show, pertaining to claims 5 and 20, including lifting off a resist to remove the copper from the catalyst.

Ramanathan teaches, in figures 4-13, and corresponding text, a method for bonding two substrates using copper-to-copper bonding where openings are between the metal pillars (paragraphs [0030], [0040-0042]).

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It would have been obvious to one of ordinary skill in the art to substitute the following steps of: including combining said (two semiconductor substrates) substrates using copper-to-copper bonding; including masking said catalyst to avoid coating the catalyst with the copper; including lifting off a resist to remove the copper from the catalyst, in the method of Jankowski, pertaining to claims 3-5 and 18-20, according to the teachings of Ramanathan, with the motivation of bonding the substrates with copper at a lower temperatures and lowering the resistance between the bonding regions of the substrates, resulting in a more efficient bonding technique. Finally, it would be obvious to protect the catalyst with a mask to avoid the copper coating, with the motivation of, only placing the copper within the bonding regions of the substrates to perform the copper to copper bonding of the two substrates.

Allowable Subject Matter

Claims 14, 16 and 17, are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Jankowski et al. Patent Application Publication US 2004/0072039, taken alone or in combination with Ramanathan et al., Patent Application Publication US 2005/0003664, fails to show the following steps:

Pertaining to independent claim 14, "protecting said catalyst when forming said channels."

Response to Arguments

Applicant's arguments filed 6/17/05 have been fully considered but they are not persuasive.

In response to the Applicant's Remarks, page 4:

Applicant raises the clear issue of whether the circulation taught by Jankowski is unnecessary and that the intrusion of a central structure to provide the U-shaped arrangement is unneeded.

The Examiner takes the position that "a channel that extends completely through at least one of said substrates" and "the fluid circulation from one side to the other." is not claimed. The claim only calls for "at least one of said trenches extending completely across one of said semiconductor substrates from edge to edge;" where Jankowski teaches, a method comprising combining the substrates in face-to-face abutment with the trenches in alignment are shown, within figures 9 and 10, and paragraphs [0029] and [0044-0046]. Specifically, Jankowski teaches, that the host structures **906/908** and consists of silicon wafers that have channels (implied trenches) etched within the silicon wafers, and are bonded together to form flow channels.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
June 26, 2005



LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812